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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/336,090	06/18/1999	FRANK KASTENHOLZ	AGM-006	7246

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EXAMINER	
LY, ANH VU H	

ART UNIT	PAPER NUMBER
2667	14

DATE MAILED: 04/16/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/336,090	KASTENHOLZ ET AL.	
	Examiner	Art Unit	
	Anh-Vu H Ly	2667	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 January 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *21* is/are allowed.

6)☒ Claim(s) *1-9,11,13-16,18-20 and 22-26* is/are rejected.

7)☒ Claim(s) *10,12 and 17* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *18 June 1999* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *11*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. This communication is in response to applicant's amendment filed January 28, 2004. Claims 1-26 are pending.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-4, 11, 13, 15, 18-20, and 24-26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Prasad (US Patent No. 6,049,542) in view of Lyon et al (US Patent No. 5,920,705). Hereinafter, referred to as Prasad and Lyon.

With respect to claims 1, 13, 15, 20, and 24-26, Prasad discloses in Fig. 3, a scalable switch fabric architecture including a number of switching elements 111-112, 121-122, 131-132 and a replacement core stage 301 (an expanded interconnect module located proximate to local interconnect modules). Herein, the switching elements 111-112 are considered as first stage and/or input stage (local line card modules), switching elements 121-122 considered as second stage and/or core stage, and switching elements 131-132 considered as third stage and/or output stage. The outputs of first stage or input stage are connected to the switching elements 121-122 and the core stage 301. Herein, the switching elements 121-122 and core stage 301 considered as local interconnect modules (a selectable number of local interconnect modules connected to the local line card modules). As shown in Fig. 3, the switching elements are uniformly

distributed on the switch fabric architecture (located proximate to each other) and each switching element and the core stage 301 including the functional devices, not shown, for directing and switching traffic received at the inputs to the correct outputs. Herein, the solid lines connecting the outputs of switching elements 111-112 to the core stage 301, and the solid lines connecting the outputs of core stage 301 to the mux 302a-302h are considered as non-local I/O channels (coupling means for electrically coupling to non-local I/O channels). The input solid lines at the switching elements 111-112 and output solid lines at the switching elements 131-132 are considered as local I/O channels (each including local transfer elements and expanded transfer element for transferring information between a plurality of local I/O channels, transferring information between plurality of local I/O channels and a plurality of non-local I/O channels, and transferring information between local interconnect modules). Prasad does not disclose local line card modules configured to process information received at a plurality of speeds and formatted according to a plurality of protocols. Lyon discloses (col. 9, lines 6-30 and Figs. 1A-C and 2A-C) a packet switching network comprising a plurality of switching gateway units 21 serving as an access device to enable connection of existing LAN and backbone environments to a network of basic switching units. Each of the switching gateway unit including a gateway switch controller; whereby each gateway switch controller including multiple network adaptors or NICs 27 (local line card modules) and an ATM NIC 29 (local line card module). Accordingly, NICs 27 may be of different types, such as for example 10BaseT Ethernet NICs, 100BaseT Ethernet NICs, FDDI NICs, and others, or any combination of the preceding. Herein, Ethernets, FDDI, and ATM are known to have different transmission speeds (a plurality of local line card modules configured to process information received at a plurality of speeds and

formatted according to a plurality of protocols). It would have been obvious to one having ordinary skill in the art at the time the invention was made to include the feature of receiving information at a plurality of speeds and formatted at a plurality of protocols in Prasad's system, as suggested by Lyon, to serve the existing LAN to the high-speed backbone networks.

With respect to claims 2-3, Prasad discloses in Fig. 3, scalable multistage interconnection network architecture such as a router or a switch for switching traffic in a communications network. Prasad does not disclose wherein said local transfer elements and expanded transfer element including means for synchronizing information transferred between each of said local transfer elements". However, synchronization within a switching system is well known in the art. It would have been obvious to one having ordinary skill in the art at the time the invention was made to include synchronization in Prasad's system, to synchronize data movements between switching elements.

With respect to claim 4, Prasad discloses in Fig. 5, a flow diagram illustrating a process of upgrading the scalable switch fabric architecture (hot-swap means for changing the selected number of local interconnect modules included in the interconnect network, while the interconnect network is transferring information).

With respect to claim 11, Prasad discloses in Fig. 3, scalable multistage interconnection network architecture. Prasad does not disclose redundancy generating means for generating an alternative version of information being transferred out of the interconnect network through local

I/O channels. It is known in the art in a multicasting or broadcasting network, information received is duplicated for transferring to multiple destinations. It would have been obvious to one having ordinary skill in the art at the time the invention was made to include duplicative means for duplicating information in Prasad's system, to transfer information to multiple destinations simultaneously.

With respect to claim 18, Prasad discloses in Fig. 4, that the core stage 301 is identical to the switching units 121-122 of Fig. 3 (local transfer elements and expanded transfer elements are substantially identical).

With respect to claim 19, Prasad discloses in Fig. 5, a flow diagram showing when the transfer elements of the core stage 301 is implemented over the transfer elements of the switching units 121-122 (local and expanded transfer elements each includes mode control means for selecting whether transfer element is to be employed in one of local interconnect modules or in expanded interconnect module).

3. Claims 5, 14, and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Prasad (US Patent No. 6,049,542) and Lyon et al (US Patent No. 5,920,705) in view of Bass et al (US Patent No. 6,052,375). Hereinafter, referred to as Prasad, Lyon, and Bass.

With respect to claim 5, Prasad and Lyon have addressed all the limitations recited in parent claim 1. Prasad does not disclose wherein local I/O channels have an associated priority and the interconnect network further comprising QoS means for transferring information from

one of local I/O channels having a relatively higher priority in preference to transferring information from one of local I/O channels having a relatively lower priority. Bass discloses in Fig. 5, a high level flow chart of the port priority (channel priority) arbiter for selecting data to be transferred via the high-speed internetworking device. It would have been obvious to one having ordinary skill in the art at the time the invention was made to include the port priority arbiter in Prasad's system, as suggested by Bass, for traffic shaping in the internetworking device.

With respect to claims 14 and 16, Prasad and Lyon have addressed all the limitations recited in parent claim 1. Prasad does not disclose a memory queue for intermediately storing plurality of information cells to be transferred and queue detection means for detecting when a selected number of information cells are stored in the memory queue, wherein said local transfer elements are adapted for transferring plurality of information cells in response to queue detection means detecting storing of selected number of information cells. Bass discloses in Fig. 9, a block diagram of high-speed traffic scaler and shaper including a number of queues for storing information, queue allocation manager for allocating queues, queue priority arbiter for detecting priority of information and transferring information over internetworking device. It would have been obvious to one having ordinary skill in the art at the time the invention was made to include the queues, queue allocation manager, queue priority arbiter in Prasad's system, as suggested by Bass, for traffic shaping in the internetworking device.

4. Claims 6-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Prasad (US Patent No. 6,049,542) and Lyon et al (US Patent No. 5,920,705) in view of Fan et al (US Patent No. 6,408,005). Hereinafter, referred to as Prasad, Lyon, and Fan.

With respect to claims 6-9, Prasad and Lyon have addressed all the limitations recited in parent claim 1. Prasad does not disclose wherein local I/O channels have an associated availability for receiving information; the interconnect network further comprising status means for maintaining a status indicative of the associated availability for one or more of local I/O channels, back pressure means for communicating the status out of the local I/O channels; local interconnect modules including a plurality of memory queues, plurality of local I/O channels having associated memory queues; and memory queues having means for storing information received by way of on associated local I/O channel. Fan discloses (col. 4, lines 38-41) that when a buffer reaches its limit, a backpressure signal is sent to the source. Upon receiving the signal the source would stop transmission until the buffer signals that the pressure was relieved. Fan further discloses in Fig. 2 each stream i has a queue, Q1-QN, for storing information. It would have been obvious to one having ordinary skill in the art at the time the invention was made to include backpressure mechanisms and queues for storing information in Prasad's system, as suggested by Fan, for reducing traffic congestion in the switching unit.

5. Claim 22 is rejected under 35 U.S.C. 103(a) as being unpatentable over Prasad (US Patent No. 6,049,542) in view of Yin (US Patent No. 6,219,728).

With respect to claim 22, Prasad discloses in Fig. 3, a scalable switch fabric architecture including a number of switching elements 111-112, 121-122, 131-132 and a replacement core

stage 301 (an expanded interconnect module). Herein, the switching elements 111-112 are considered as first stage and/or input stage (local line card modules), switching elements 121-122 considered as second stage and/or core stage, and switching elements 131-132 considered as third stage and/or output stage. The outputs of first stage or input stage are connected to the switching elements 121-122 and the core stage 301. Herein, the switching elements 121-122 and core stage 301 considered as local interconnect modules (a selectable number of local interconnect modules). Each switching element and the core stage 301 including the functional devices, not shown, for directing and switching traffic received at the inputs to the correct outputs. Herein, the solid lines connecting the outputs of switching elements 111-112 to the core stage 301, and the solid lines connecting the outputs of core stage 301 to the mux 302a-302h are considered as non-local I/O channels (coupling means for electrically coupling to non-local I/O channels). The input solid lines at the switching elements 111-112 and output solid lines at the switching elements 131-132 are considered as local I/O channels (each including local transfer elements and expanded transfer element for transferring information between a plurality of local I/O channels, transferring information between plurality of local I/O channels and a plurality of non-local I/O channels, and transferring information between local interconnect modules). Prasad does not disclose quality of service means for differentiating between information coupled into local I/O channels based on an associated priority of information, and for indicating unavailability for receiving information having a particular associated priority on one or more of local I/O channels. Yin discloses in Fig. 8B, the cell with an associated priority is determined to be discarded or not upon receiving an indication of discard threshold and address queue usage by the discard determiner. It would have been obvious to one having ordinary skill in the art at the

time the invention was made to include the feature of indicating the status of the memory associated with cell priority in Prasad's system, as suggested by Yin, to reduce overload or congestion within the switching network.

6. Claim 23 is rejected under 35 U.S.C. 103(a) as being unpatentable over Prasad (US Patent No. 6,049,542) in view of Rathnavelu (US Patent No. 5,751,709).

With respect to claim 23, Prasad discloses in Fig. 3, a scalable switch fabric architecture including a number of switching elements 111-112, 121-122, 131-132 and a replacement core stage 301 (an expanded interconnect module). Herein, the switching elements 111-112 are considered as first stage and/or input stage (local line card modules), switching elements 121-122 considered as second stage and/or core stage, and switching elements 131-132 considered as third stage and/or output stage. The outputs of first stage or input stage are connected to the switching elements 121-122 and the core stage 301. Herein, the switching elements 121-122 and core stage 301 considered as local interconnect modules (a selectable number of local interconnect modules). Each switching element and the core stage 301 including the functional devices, not shown, for directing and switching traffic received at the inputs to the correct outputs. Herein, the solid lines connecting the outputs of switching elements 111-112 to the core stage 301, and the solid lines connecting the outputs of core stage 301 to the mux 302a-302h are considered as non-local I/O channels (coupling means for electrically coupling to non-local I/O channels). The input solid lines at the switching elements 111-112 and output solid lines at the switching elements 131-132 are considered as local I/O channels (each including local transfer elements and expanded transfer element for transferring information between a plurality of local

I/O channels, transferring information between plurality of local I/O channels and a plurality of non-local I/O channels, and transferring information between local interconnect modules). Prasad does not disclose local and expanded transfer elements include clumping means for substantially simultaneously transferring a plurality of information cells. Rathnavelu discloses in Tables 1-3, how cells are clumped to arrive an acceptable cluster size. It would have been obvious to one having ordinary skill in the art at the time the invention was made to include the clumping means in Prasad's system, as suggested by Rathnavelu, to arrive an acceptable cluster size.

Response to Arguments

7. Applicant's arguments with respect to claims 1-26 have been considered but are moot in view of the new ground(s) of rejection.

Allowable Subject Matter

8. Claims 10, 12, and 17 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. The prior art does not teach or fairly suggest wherein backpressure means is adapted for replacing said destination address portion with said status for communication said status out of said interconnect network, as specified in dependent claim 10. The prior art does not teach or fairly suggest wherein redundancy generating means is adapted for causing said alternative version of said information to be a bit by bit "exclusive-or" between pairs of said groups of information words included in an information cell, as specified in dependent claim 12. The prior art does not teach or fairly suggest the expanded interconnect module including array means for storing path information representative of a plurality of paths

through said expanded transfer elements over which information from a first local I/O channel of one of said local interconnect modules can be transferred to a second local I/O channel of another one of said local interconnect modules and index means for selecting appropriate path information from said array means, at least partially in response to a destination address of said second local I/O channel, as specified in dependent claim 17.

9. Claim 21 is allowed.

The following is an examiner's statement of reasons for allowance:

The prior art does not teach or fairly suggest redundancy generating means for generating an alternative version of information being transferred out of said interconnect network by generating a bit-by-bit "exclusive-or" between pairs of said groups of information words included in an information cell, as specified in independent claim 21.

Conclusion

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Anh-Vu H Ly whose telephone number is 703-306-5675. The examiner can normally be reached on Monday-Friday 7:00am - 4:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chi Pham can be reached on 703-305-4378. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

avl

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